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ELECTRO-ALLOYS CORP.

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LOW STRESS HIGH RELIABILITY LIDS FOR SEMICONDUCTOR PACKAGES

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Introduction

Metal alloy lids used for the hermetic sealing of ceramic multilayer semiconductor packages are almost invariably fabricated from F-15 alloy (Kovar®, Sealvar®) or Alloy 42. The base metal lids are nickel and gold plated and then usually sealed to the metalized seal ring of the ceramic package with gold-tin eutectic alloy solder (80% gold, 20% tin). Such relatively expensive packages are primarily used for semiconductor devices which are incorporated into military equipment and where very high reliability is mandated. The multilayer ceramic body is manufactured from 90% to 92% opaque alumina.

The first packages of this construction, predominantly of the dual-inline type, came into use about 1964 which is a few years after the invention of the integrated circuit. At that time both Kovar® and Alloy 42 were being used for glass-to-metal seals and were generally available at a reasonable cost. Because the integrated circuit silicon chips were relatively small and were soldered into a small cavity of the ceramic package, the lids used to complete the hermetic seal were small in dimensions - the maximum dimension not exceeding one-half inch. The difference in the linear thermal coefficients of expansion between the ceramic of the package body and the metal lid was small enough for the small sized cavity so that no significant stress developed at the solder junction of the lid and the seal ring of the package. Almost all dual-inline packages had a Kovar seal ring preform brazed to the ceramic around the chip cavity. Because the T.C.E. of the seal ring and the lid matched, this further justified the use of Kovar for fabrication of the lids. Later, the Kovar seal ring was replaced by the metalization of a seal ring area around the cavity.

Over the years the integrated circuit chips have dramatically increased in complexity with the chip dimensions becoming much larger and requiring many more bonding pads within the cavity of the package. This has necessitated a much larger chip cavity in the package and a much larger mating lid for the hermetic sealing of the cavity. Until a few years ago lids were seldom above three-

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quarters of an inch for the maximum dimension and lead count was seldom above thirty-six in number. Now, lids are often above one inch on a side and leads may number in the hundreds for pin grid array packages.

As larger lids have come into use the difference in the linear thermal coefficients of expansion of the ceramic and Kovar or Alloy 42 has become significant in introducing large stresses at the solder seal between the metal lid and the ceramic body. This stress has become large enough for lids having a dimension exceeding one inch in length to make the integrity of the gold-tin solder seal questionable. However, semiconductor manufacturers have not changed their procurement specifications for lids and their procurement drawing still specify the lid alloy to be Kovar or either Kovar or Alloy 42.

High Reliability, Low Stress Lids

From an investigation of which alloys conform to military specifications and which have significantly closer coefficients of thermal expansion to the ceramic body than Kovar or Alloy 42, it is noted that Alloy 45 (45% nickel, remainder iron) has a coefficient much closer to the ceramic over the temperature range of interest. All other mechanical and physical properties are nearly the same. The accompanying graphs show the linear thermal coefficients of Kovar, Alloy 42, Alloy 45 and Alloy 46. Much of this data was supplied by Ametek, Carpenter Steel, Kyocera and NTK. The temperature range of 30°C to 300°C is of most significance because it is the dominating range over which the stress at the solder seal is developed. Gold-tin eutectic of 80% gold and 20% tin has a solidus temperature of 280°C. The solder preforms are usually supplied with 79.3% gold and 20.7% tin. When the solder liquifies during the sealing operation, gold plating on the lid and on the seal ring alloy with the solder and bring the alloy very close to 80% gold and 20% tin composition.

Military specifications call for either Kovar or Alloy 42 for the metal parts such as ladder frames and interconnect pins which are brazed to the ceramic body. They do not specifically designate these two alloys for the lid. Iron-nickel alloys are listed in MIL-I-23011C which are used for sealing metal to glass and to ceramic. Both Alloy 45 and Alloy 46 conform to alloys as being acceptable.

Referring to the graphs over the temperature range of 30°C to 300°C, 91% opaque alumina has a thermal coefficient of expansion of 6.8×10^{-6}/°C, Kovar 5.2×10^{-6}/°C and Alloy 45 has a coefficient of

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6.6 x 10^{-6}/°C. Alloy 45 has the closest thermal expansion match to ceramic from which the package body is fabricated. It will therefore induce significantly lower stresses at the gold-tin solder seal than will either Kovar or Alloy 42. Since the modulus of elasticity of the ceramic is much greater than the modulus of the metal lid, it can be assumed that the lidded package will remain essentially undistorted after the package sealing operation has been completed. For large lids- over three-quarters of an inch square- the thickness of the lid is usually fifteen thousandths of an inch. Stress in the lid may cause a slight "oil-canning" distortion of the lid but the degree of distortion is very difficult to predict. As a rough approximation, the stress on the solder seal will be directly proportional to the differences of the linear thermal coefficients of expansion between the ceramic and the various alloy lids. For Kovar the difference is 1.6 x 10^{-6}/°C and for Alloy 45 is 0.2 x 10^{-6}/°C. This means that the stress on the solder seal will be roughly eight times greater for Kovar® than for Alloy 45. It will be even greater for Alloy 42.

Conclusion

Because of the recent increase in the size of lids and thickness of the solder preforms which are specified by manufacturers to hermetically seal multilayer semiconductor packages, excessive stress is being generated at the solder seal between the lid and the seal ring of the package. For lids above one inch in size the stress becomes great enough to make doubtful the integrity of the seal and therefore the long term reliability of the semiconductor device.

The cause of the excessive stress at the seal is the mismatch of the linear thermal coefficient of expansion between ceramic of the package and either Kovar or Alloy 42 which are invariably specified as the required alloys for the lid.

Alloy 45 has a much better thermal coefficient match than Kovar or Alloy 42 and should be considered by manufacturers as the alloy to be used in fabricating the lid. Any increase in hermetic sealing yields for ASIC's and MPU's well justifies the change. Alloy 45 conforms to military specifications, is generally available and should be in the same price range as Alloy 42 and possibly lower in cost than Kovar.

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Linear Thermal Coefficient of Expansion