Materials in Electronic Manufacturing: Electronic Packaging

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History of Electronic Packaging

Electronic packaging involves using an appropriate combination of conductive and dielectric materials to electrically interconnect and mechanically support electronic components in a reliable and cost-effective manner. Since the invention of the integrated circuit in 1959 and mass wave-soldering in 1958,[1] the vast majority of electronic packaging has involved a planar substrate to which semiconductor devices in protective packages are attached by melting eutectic solder. The planar substrates or printed circuit boards (PCBs) were invented in 1940,[2] but their widespread implementation was limited until the invention of mass soldering. PCBs use conventional epoxy-glass dielectric material with mass patterned conductive traces of copper, but alternative materials have been used for either enhanced electrical performance or lower product cost.

The ever-increasing complexity of integrated circuits requires a similar increase in the number of leads or interconnections to access the circuit. This ever-increasing need for interconnections has been a driving force for advances in electronic packaging technology. The complexity of an integrated circuit is measured by the number of electronic functions or gates it contains. Rent's rule predicts that for random logic the number of leads, n, can be estimated from the number of gates, g, by:

$$n = c(g)^{\beta} \qquad (1)$$

where for gate arrays,[3] $c = 1.9$ and $\beta = 0.5$.

Until the 1980s, integrated circuits were typically packaged in dual-in-line packages with up to 64 leads inserted in plated-through-holes that pierced the printed circuit board (PCB) (Figure 1). Electrical and mechanical attachment was achieved by passing the assembly through a fountain or "wave" of molten tin-lead solder. Manufacturing defects were typically 4% or 40,000 ppm. This defect level, however, was largely determined by the time-study engineer who specified the appropriate number of workers to touch up 4% of the soldered interconnections. Management had not established an independent goal for expected quality; they did not recognize that they had allowed the time-study engineer to establish quality expectations.

Introduction of Surface Mount Technology

During the late 1980s a significant change took place in electronic packaging, driven by the need for more leads, reduced size, faster electrical performance, and increased heat dissipation. Instead of using plated-through-holes on a 2.5 mm pitch, the new surface-mount-technology, high-density components were typically square and had peripheral leads soldered to conductive pads on the surface of the PCB. Components now could be placed on both sides of the board and there were no large plated-through holes to restrict space for routing the wiring. From a design perspective, there was no change in the material system, but significant increase in the packaging density. The PCB now was a multilayered PCB with internal circuitry to increase interconnectivity (Figure 2).

From a manufacturing perspective, there was a significant change in process and materials. Typically, the complex components had 60 to 200 leads with pitches down to 0.5 mm. Precise component placement equipment with sophisticated vision systems was developed. The components could no longer be attached by

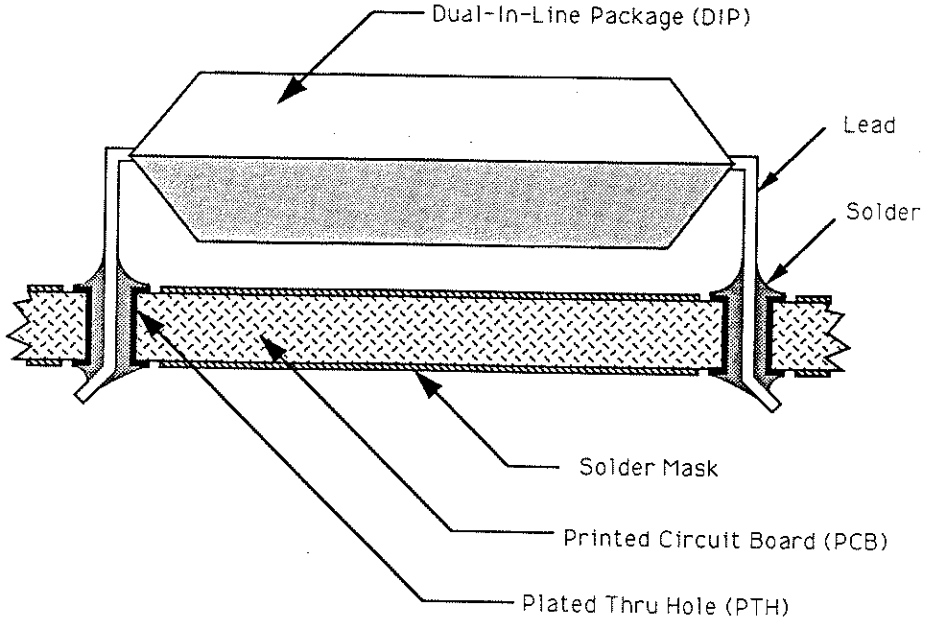

Figure 1. Dual-in-line package on printed circuit board, c. 1970.

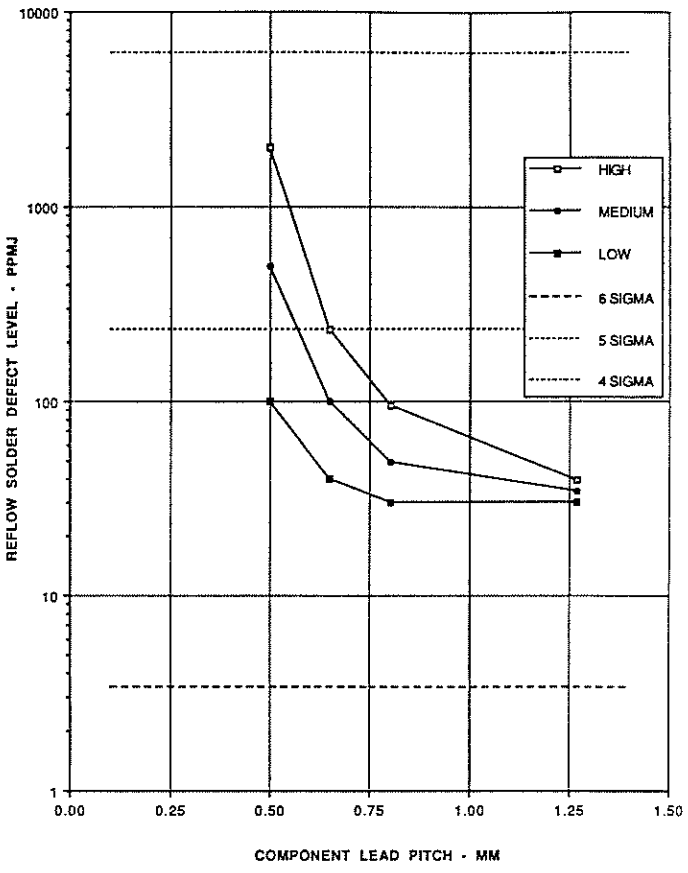

Figure 3. Reflow soldering process yield vs. lead pitch for quad flat packs (QFPs).

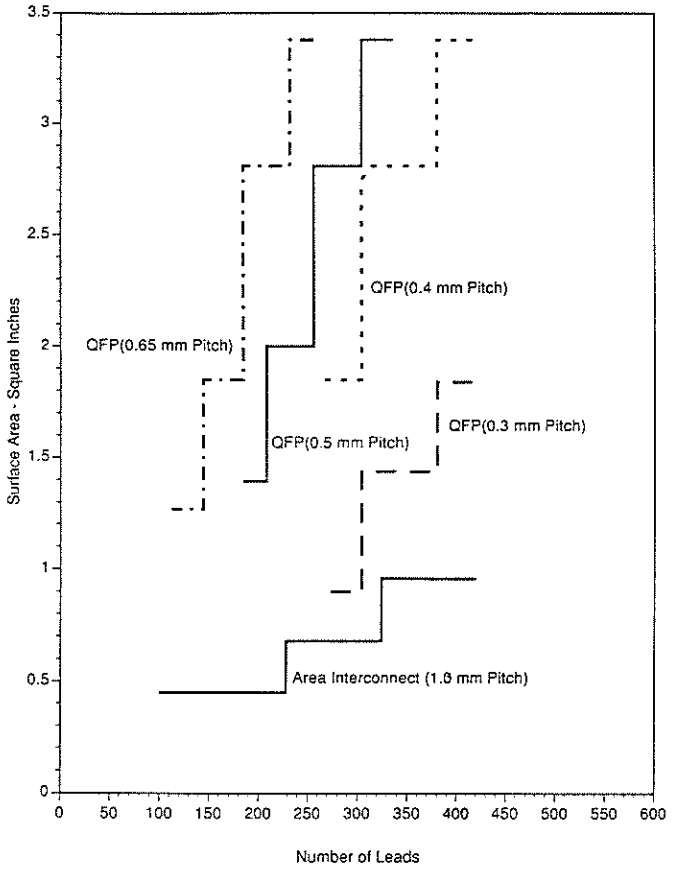

Figure 4. Surface area vs. number of leads.

This tradeoff is illustrated in Figure 4, which shows the size of an area array package of 1.0 mm pitch versus 0.3 to 0.65 mm pitch quad flat packs. The conventional wisdom is that area interconnections are not acceptable because they cannot be inspected. But if you can achieve *Six Sigma* quality, then you do not need to inspect the solder interconnections! So the goal was to develop a design using appropriate materials for reliability and appropriate processes to ensure achieving *Six Sigma* quality.

First-Generation Solution

The initial application of the solution was in Motorola's HyperModule™ RISC microcomputer system. The solution involved packaging the RISC (reduced instruction set computer) microprocessor in a multilayer co-fired ceramic package (Figure 5).[15] The package has an array of 285 gold-plated metalized pads on 1.6 mm pitch on the bottom surface. A solder ball, 0.75 mm in diameter, is fused to each of these pads. The process to attach this package to a printed circuit board involved no change from the existing manufacturing process, materials, or equipment. Volume production has demonstrated that this process exceeds *Six Sigma* quality by achieving 3.0 ppm defective joints.

There was one drawback to this solution—cost-effective reliability. The solder interconnections are subject to an end-of-life failure from solder fatigue after a number of thermal cycles. There are well-defined empirical formulas to determine the life expectancy.[16] Major parameters affecting the fatigue life include the coefficient of thermal expansion mismatch between the PCB and the package, the distance between the PCB and the package, and the fatigue resistance of the chosen solder. For the HyperModule™ design, it was necessary to embed two copper-invar-copper layers within the PCB to match the thermal expansion coefficient of the PCB with the package. This design choice, while meeting all system requirements, increased the cost of the product and limited the number of PCB vendors.

Second-Generation Solution

The second-generation design increased the capabilities of the area interconnect technology through improved choices of materials for manufacturability and quality. The new design, shown in Figure 6, provides for 324 leads on a 1 mm array pitch. With the improved package design, Motorola achieves 56% more interconnections in 48% of the area required by a quad flat pack. The new co-fired package design involves four conductive layers instead of nine in the previous design; these design improvements significantly reduce

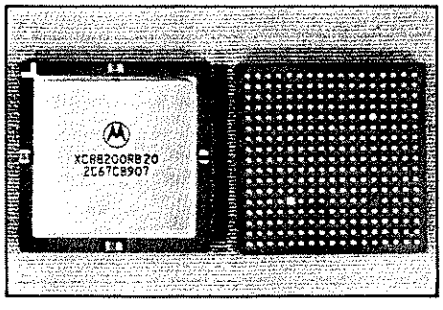

Figure 5. Photograph of RISC microprocessor area array package with 285 leads.